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L8: Entry 1 of 4

File: PGPB

Nov 14, 2002

PGPUB-DOCUMENT-NUMBER: 20020169945

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020169945 A1

TITLE: Microprocessor

PUBLICATION-DATE: November 14, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Haraguchi, Yoshiyuki	Tokyo		JP	

US-CL-CURRENT: 712/205; 712/234, 712/241

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KIMC	Draw De
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☐ 2. Document ID: US 20020083312 A1

L8: Entry 2 of 4

File: PGPB

Jun 27, 2002

PGPUB-DOCUMENT-NUMBER: 20020083312

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020083312 A1

TITLE: Branch Prediction apparatus and process for restoring replaced branch history for use in future branch predictions for an executing program

PUBLICATION-DATE: June 27, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Sinharoy, Balaram	Poughkeepsie	NY	US	

US-CL-CURRENT: 712/240

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KIMC	Draw De
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☐ 3. Document ID: US 6745320 B1

L8: Entry 3 of 4

File: USPT

Jun 1, 2004

US-PAT-NO: 6745320

DOCUMENT-IDENTIFIER: US 6745320 B1

TITLE: Data processing apparatus

Full	Title	Citation	Front	Review	Classification	Date	Reference	Abstracts	Attachments	Claims	KWIC	Draw De
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☐ 4. Document ID: US 5333280 A

L8: Entry 4 of 4

File: USPT

Jul 26, 1994

US-PAT-NO: 5333280

DOCUMENT-IDENTIFIER: US 5333280 A

TITLE: Parallel pipelined instruction processing system for very long instruction word

Full	Title	Citation	Front	Review	Classification	Date	Reference	Abstracts	Attachments	Claims	KWIC	Draw De
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☐ 1. Document ID: US 6745320 B1

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L13: Entry 1 of 10

File: USPT

Jun 1, 2004

US-PAT-NO: 6745320

DOCUMENT-IDENTIFIER: US 6745320 B1

TITLE: Data processing apparatus

DATE-ISSUED: June 1, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Mitsuishi; Naoki	Kodaira			JP

US-CL-CURRENT: 712/225; 711/212, 711/214, 712/201, 712/202, 712/203, 712/209,
712/227, 712/245

Full	Title	Citation	Front	Review	Classification	Date	Reference	Attachments	Attachments	Claims	KMC	Draw De
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☐ 2. Document ID: US 6738893 B1

L13: Entry 2 of 10

File: USPT

May 18, 2004

US-PAT-NO: 6738893

DOCUMENT-IDENTIFIER: US 6738893 B1

TITLE: Method and apparatus for scheduling to reduce space and increase speed of microprocessor operations

Full	Title	Citation	Front	Review	Classification	Date	Reference	Attachments	Attachments	Claims	KMC	Draw De
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☐ 3. Document ID: US 6615339 B1

L13: Entry 3 of 10

File: USPT

Sep 2, 2003

US-PAT-NO: 6615339

DOCUMENT-IDENTIFIER: US 6615339 B1

TITLE: VLIW processor accepting branching to any instruction in an instruction word

h e b b g e e f e ef b e

set to be executed consecutively

Full	Title	Citation	Front	Review	Classification	Date	Reference	Attachments	Claims	KMC	Drawings
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☐ 4. Document ID: US 6564316 B1

L13: Entry 4 of 10

File: USPT

May 13, 2003

US-PAT-NO: 6564316

DOCUMENT-IDENTIFIER: US 6564316 B1

TITLE: Method and apparatus for reducing code size by executing no operation instructions that are not explicitly included in code using programmable delay slots

Full	Title	Citation	Front	Review	Classification	Date	Reference	Attachments	Claims	KMC	Drawings
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☐ 5. Document ID: US 6370638 B1

L13: Entry 5 of 10

File: USPT

Apr 9, 2002

US-PAT-NO: 6370638

DOCUMENT-IDENTIFIER: US 6370638 B1

TITLE: Apparatus and method of computer program control in computer systems using pipeline processing

Full	Title	Citation	Front	Review	Classification	Date	Reference	Attachments	Claims	KMC	Drawings
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☐ 6. Document ID: US 6324639 B1

L13: Entry 6 of 10

File: USPT

Nov 27, 2001

US-PAT-NO: 6324639

DOCUMENT-IDENTIFIER: US 6324639 B1

TITLE: Instruction converting apparatus using parallel execution code

Full	Title	Citation	Front	Review	Classification	Date	Reference	Attachments	Claims	KMC	Drawings
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☐ 7. Document ID: US 6275929 B1

L13: Entry 7 of 10

File: USPT

Aug 14, 2001

US-PAT-NO: 6275929

DOCUMENT-IDENTIFIER: US 6275929 B1

TITLE: Delay-slot control mechanism for microprocessors

Full	Title	Citation	Front	Review	Classification	Date	Reference	Abstracts	Attachments	Claims	KWIC	Draw De
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☐ 8. Document ID: US 5958044 A

L13: Entry 8 of 10

File: USPT

Sep 28, 1999

US-PAT-NO: 5958044

DOCUMENT-IDENTIFIER: US 5958044 A

TITLE: Multicycle NOP

Full	Title	Citation	Front	Review	Classification	Date	Reference	Abstracts	Attachments	Claims	KWIC	Draw De
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☐ 9. Document ID: US 5581778 A

L13: Entry 9 of 10

File: USPT

Dec 3, 1996

US-PAT-NO: 5581778

DOCUMENT-IDENTIFIER: US 5581778 A

TITLE: Advanced massively parallel computer using a field of the instruction to selectively enable the profiling counter to increase its value in response to the system clock

Full	Title	Citation	Front	Review	Classification	Date	Reference	Abstracts	Attachments	Claims	KWIC	Draw De
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☐ 10. Document ID: US 5398321 A

L13: Entry 10 of 10

File: USPT

Mar 14, 1995

US-PAT-NO: 5398321

DOCUMENT-IDENTIFIER: US 5398321 A

TITLE: Microcode generation for a scalable compound instruction set machine

Full	Title	Citation	Front	Review	Classification	Date	Reference	Abstracts	Attachments	Claims	KWIC	Draw De
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L12 (712/245)[CCLS]	490	L12
L11 (712/245)![CCLS]	490	L11
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L7 L6 and l1	16	L7

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<u>L5</u>	L4 and l2	57	<u>L5</u>
<u>L4</u>	(NOP or (("no" or iddle) near2 operation\$1)) near15 (branch or conditional or instruction) near5 (field\$1 or portion\$1)	218	<u>L4</u>
<i>DB=PGPB,USPT; PLUR=YES; OP=OR</i>			
<u>L3</u>	L2 and l1	70	<u>L3</u>
<u>L2</u>	(712/221-300)! [CCLS]	4658	<u>L2</u>
<i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>			
<u>L1</u>	(NOP or (("no" or iddle) near2 operation\$1)) near15 (branch or conditional or instruction) near5 (field\$1 or portion\$1 or format)	256	<u>L1</u>

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Computers, IEEE Transactions on , Volume: 48 , Issue: 5 , May 1999

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Pawlovsky, A.P.; Hanawa, M.;

Test Symposium, 1992. (ATS '92), Proceedings., First Asian (Cat. No.TH04580) , 26-27 Nov. 1992

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Edwards, S.A.;

Hardware/Software Codesign, 1999. (CODES '99) Proceedings of the Seventh International Workshop on , 3-5 May 1999

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Computers, IEEE Transactions on, Volume: 48, Issue: 5, May 1999

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